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10/763,043	01/21/2004	Weimin Zhang	019927-001810US	3805

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TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
BOCURE, TESFALDET	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/763,043	ZHANG ET AL.	
	Examiner	Art Unit	
	Tesfaldet Bocure	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) *23-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/12/04, 3/12/07 & 7/16/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 are pending in the Application.

Information Disclosure Statement

2. The Examiner has approved the received Information Disclosure Statements on 3/12/07 and 7/16/07 and the initialed copies y (four pages) of the 1449 are attached with this correspondence. In the meantime, the IDSs of 7/12/04 were not cuptured in the eDan and examiner is resubmitting the partially signed IDSs incase Applicant did not receive them. It should be noted that one page from the IDSs received on 7/12/04 is a duplicate copy and has not been considered by the Examiner.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claimed "down-sample circuit" in claim 23 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet,

and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.
It should be noted that the best figure describing the claimed invention is figure 4 and the down-sampling is not showing.

Claim Objections

4. Claims 23-27 are objected to because of the following informalities: the claimed "plurality of low-pass filters and a discrete Fourier transform circuit" in claim 23 should be clearly recited as being responsive to the 'down-sampler.' Appropriate correction is required.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140

F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1-20 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-19 of U.S. Patent No. 6,704,372. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claimed invention in the instant application differs from that of the US patent number 6,704,372 that the selector has been claimed in claim 2, which depends on claim 1 of the instant application while in claim 1 in the US patent number 6,704,372 and as shown by highlighted comparison below.

It should be noted that the "one or more demodulators configured to receive and demodulate one or more ***digital RF channels <u>selected</u> from the plurality of separate digital RF channels*** claimed in claim 1 of the instant application is silently claiming as that of the selector in claim 1 in the US patent 6,704,372.

US patent Application No. 10/763,043 (Instant Application)	US patent number 6,704,372

1. A digital multi-channel demodulator circuit for processing a multi-channel analog RF signal, the multi-channel demodulator comprising: a frequency-block down-converter configured to receive the analog RF signal and to shift the analog RF signal to a lower frequency band; an analog-to-digital converter (ADC) configured to receive the analog RF signal from the frequency-block down-converter and to convert the analog RF signal to a multi-channel digital RF signal; a digital channel demultiplexer configured to receive the digital RF signal from the ADC and to demultiplex the digital RF signal into a plurality of separate digital RF channels; and one or more demodulators configured to receive and demodulate one or more digital RF channels selected from the plurality of separate digital RF channels. 2. The circuit of claim 1 further comprising: ***a selector configured to receive the plurality of separate digital RF channels from the***	1. A digital multi-channel demodulator circuit for processing a multi-channel analog RF signal, the multi-channel demodulator comprising: a frequency-block down-converter configured to receive the analog RF signal and to shift the analog RF signal to a lower frequency band; an analog-to-digital converter (ADC) configured to receive the analog RF signal from the frequency-block down-converter and to convert the analog RF signal to a multi-channel digital RF signal; a digital channel demultiplexer configured to receive the digital RF signal from the ADC and to demultiplex the digital RF signal into separate digital RF channels***; a selector configured to receive the separate digital RF channels and to select one or more separate digital RF channels***; and one or more demodulators configured to receive one or more of the selected digital RF channels from the selector and to demodulate the one or more selected digital RF channels.

digital channel demultiplexer and to select the one or more digital RF channels to be received by the one or more demodulators.	
3. The circuit of claim 1 wherein each separate digital RF channel comprises one or more data streams to be accessed or used by a subscriber	2. The circuit of claim 1 wherein each separate digital RF channels comprises one or more data streams to be accessed or used by a subscriber.
4. The circuit of claim 2 wherein the one or more demodulators demodulate only the RF channels that are selected by the selector.	3. The circuit of claim 1 wherein the one or more demodulators demodulate only the RF channels that are selected by the selector.
5. The circuit of claim 2 further comprising a digital transport interface configured to receive the selected RF channels from the one or more demodulators and to output the selected RF channels.	4. The circuit of claim 1 further comprising a digital transport interface configured to receive the selected RF channels from the one or more demodulators and to output the selected RF channels.
6. The circuit of claim 1 further comprising a bandpass filter to reduce aliasing from unwanted signals.	5. The circuit of claim 1 further comprising a bandpass filter to reduce aliasing from unwanted signals.
7. The circuit of claim 1 wherein the ADC is a high-speed ADC.	6. The circuit of claim 1 wherein the ADC is a high-speed ADC.
8. The circuit of claim 1 wherein the ADC converts an entire signal band, the signal	7. The circuit of claim 1 wherein the ADC converts an entire signal band, the signal band

band including the multi-channel analog RF signal.	including the multi-channel analog RF signal.
9. The circuit of claim 1 wherein the one or more demodulators share resources.	8. The circuit of claim 1 wherein the one or more demodulators share resources.
10. The circuit of claim 1 wherein the digital channel demultiplexer includes a digital tuner.	9. The circuit of claim 1 wherein the digital channel demultiplexer includes a digital tuner.
11. The circuit of claim 10 wherein the digital tuner comprises: a numeric control oscillator (NCO) configured to generate a select frequency, the select frequency being associated with a corresponding RF channel; a complex multiplier configured to receive the digital RF signal and to multiply the digital RF signal with the select frequency; and a low-pass filter (LPF) configured to receive the digital RF signal and to pass the corresponding RF channel.	10. The circuit of claim 9 wherein the digital tuner comprises: a numeric control oscillator (NCO) configured to generate a select frequency, the select frequency being associated with a corresponding RF channel; a complex multiplier configured to receive the digital RF signal and to multiply the digital RF signal with the select frequency; and a low-pass filter (LPF) configured to receive the digital RF signal and to pass the corresponding RF channel.
12. The circuit of claim 11 wherein the LPF is a high-speed finite impulse response (FIR) filter.	11. The circuit of claim 10 wherein the LPF is a high-speed finite impulse response (FIR) filter.
13. The circuit of claim 1 wherein the digital multi-channel demodulator circuit processes	12. The circuit of claim 1 wherein the digital multi-channel demodulator circuit processes

downstream signals in at least one of a satellite system, a terrestrial TV system., and a cable system.	downstream signals in at least one of a satellite system, a terrestrial TV system, and a cable system.
14. A system using the circuit of claim 1 in combination with memory.	13. A system using the circuit of claim 1 in combination with memory.
15. A system using the circuit of claim 1 in combination with a processor.	14. A system using the circuit of claim 1 in combination with a processor.
16. The circuit of claim 1 wherein the digital channel demultiplexer is a polyphase channel demultiplexer.	15. The circuit of claim 1 wherein the digital channel demultiplexer is a polyphase channel demultiplexer.
17. The circuit of claim 16 wherein the polyphase channel demultiplexer comprises: one or more low-pass filters (LPF) configured to receive the multi-channel digital RF signal and to synchronize the RF channels; a discrete Fourier transform circuit (DFT) configured to receive the digital RF signal and to demultiplex the digital RF signal into separate RF channels.	16. The circuit of claim 16 wherein the polyphase channel demultiplexer comprises: one or more low-pass filters (LPF) configured to receive the multi-channel digital RF signal and to synchronize the RF channels; a discrete Fourier transform circuit (DFT) configured to receive the digital RF signal and to demultiplex the digital RF signal into separate RF channels.
18. The circuit of claim 17 wherein the DFT is a combination of different fast Fourier transforms.	17. The circuit of claim 16 wherein the DFT is a combination of different fast Fourier transforms

19. The circuit of claim 17 wherein the polyphase channel demultiplexer comprises at least two LPFs, the coefficients of each LPF filters being a part of a bigger low-pass filter.	18. The circuit of claim 16 wherein the polyphase channel demultiplexer comprises at least two LPFs, the coefficients of each LPF filter being a part of a bigger low-pass filter.
20. The circuit of claim 17 wherein the LPFs are low-speed finite impulse response (FIR) filters.	19. The circuit of claim 16 wherein the LPFs are low-speed finite impulse response (FIR) filters.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claim 21 is rejected under 35 U.S.C. 102(b) as being anticipated by **Smith et al., Smith** hereinafter (US patent number 5,818,883, newly cited).

Smith teaches a multi carrier receiver (see figure 2), the receiver having a down-converting unit (214) comprising: a complex multiplier (1220) for multiplying the selected signal from the plurality of antenna having a corresponding frequency with the output of the numerically controlled oscillator (1218); and digital low pass filter (1124) for filtering the selected down converted signal as in claim 21.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable **Smith** (US patent number 5,818,883, newly cited).

11. **Smith** teaches the claimed subject matter in claim 21 and that the low pass filter being a digital filter (1224 and col. 5, lines 15-20). However he fails to show that the digital low pass filter is a high-speed finite impulse response filter (FIR) as in claim 22.

However, realization of FIR in a digital filtering is notoriously known and Examiner is taking an official notice. Therefore, it would have been obvious to one of an ordinary skill in the art to implement FIR in the digital filtering of Smith to eliminate or remove any undesired alias components (col. 5, lines 10-15) at the time the invention was made.

Response to Amendment

12. In response to Applicant's remarks that a terminal disclaimer is filed to overcome the double patent rejection to claims 1-20, there is no 'terminal disclaimer' found in the

file and the rejection is still mentioned.

13. The Applicant's arguments with respect to claims 21-22 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

14. Claims 23-27 are allowed.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tesfaldet Bocure whose telephone number is (571) 272-3015. The examiner can normally be reached on Mon-Thur (7:30a-5:00p) & Mon.-Fri (7:30a-5:00p).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tesfaldet Bocure
Primary Examiner
Art Unit 2611

T.Bocure